ABSTRACT OF THE DISCLOSURE

A refresh characteristic of a DRAM memory cell is improved and the performance of a MISFET formed in the periphery thereof and constituting a logic circuit is improved.

Each gate electrode in a memory cell area is formed of p type polycrystalline silicon, and a cap insulating film on each gate electrode and a sidewall film on the sidewall thereof are formed of a silicon oxide film. A polycrystalline silicon film formed on the gate electrodes and between the gate electrodes is polished by a CMP method, and thereby contact electrodes are formed. Also, sidewall films each composed of a laminated film of the silicon oxide film and the polycrystalline silicon film are formed on the sidewall of the gate electrodes in the logic circuit area, and these films are used as a mask to form semiconductor areas. As a result, it is possible to reduce the boron penetration and form contact electrodes in a self-alignment manner. In addition, the performance of the MISFET constituting the logic circuit can be improved.